4-bit Multiplexer/Demultiplexer Chip Set for 40-Gbit/s Optical Communication Systems

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Abstract - We have designed and fabricated a low-power 4:1 multiplexer (MUX), a 1:4 demultiplexer (DEMUX), and a 1:4 DEMUX with a clock and data recovery (CDR) circuit using undoped-emitter InP/InGaAs heterojunction bipolar transistors (HBTs). Our HBTs exhibit an f_T of about 150 GHz and an f_{max} of about 200 GHz at a collector current density of 50 kA/um^2 and a collector-to-emitter voltage of 1.2 V. The error-free operations at bit rate of up to 50 Gbit/s have been confirmed for the 4:1 MUX and 1:4 DEMUX, which dissipates 2.5 W and 2.6 W, respectively. In addition, 40-Gbit/s error-free operation for the full clock rate 1:4 DEMUX with the CDR has been achieved for the first time.

I. INTRODUCTION

The multiplexer (MUX) and demultiplexer (DEMUX) are key components of optical communication systems and measuring equipment. Considerable work related to the design and fabrication of over-40-Gbit/s-class MUX and DEMUX have been carried out using InP-based heterojunction bipolar transistors (HBTs) [1]-[2], SiGe-based HBTs [3]-[5], and InP-based high electron mobility transistors (HEMTs) [6]-[7].

InP-based HBTs offer high internal gain and excellent high-frequency performance. In addition, we have already developed undoped-emitter InP/InGaAs HBT technology [8]-[9]. The undoped-emitter structure offers higher cutoff frequency f_T than the conventional n-doped-emitter one at low collector current density. Thus, undoped-emitter InP/InGaAs HBTs are potentially attractive for high-speed high-sensitivity integrated circuits (ICs) with low-power consumption. In this work, we employed undoped-emitter InP/InGaAs HBT technology to fabricate a 4:1 MUX, 1:4 DEMUX, and a full clock rate 1:4 DEMUX with clock and data recovery (CDR) circuit for over-40-Gbit/s optical communication systems and measuring equipment. We report the circuit design and experimental results for the 4-bit MUX/DEMUX chip set.

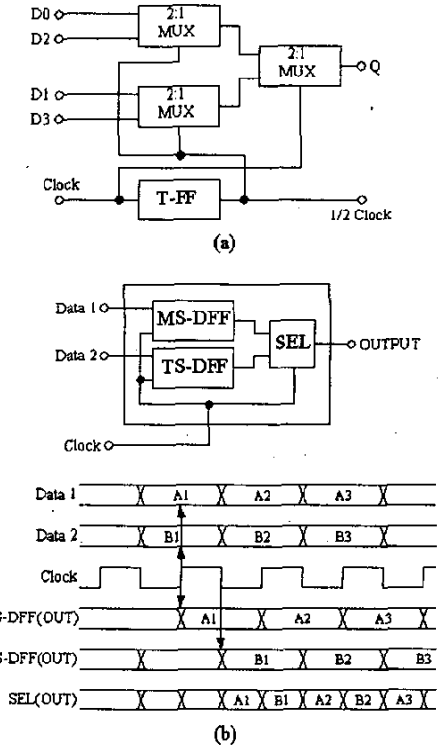

Figure 1. 4:1 MUX IC. (a) 4:1 MUX architecture. (b) 2:1 MUX block and the timing chart.

II. CIRCUIT DESIGN

A. 4:1 MUX

Fig. 1 is a schematic of the 4:1 MUX. We adopt the conventional tree-type architecture. The 2:1 MUX block consists of a three-stage D flip-flop (TS-DFF),

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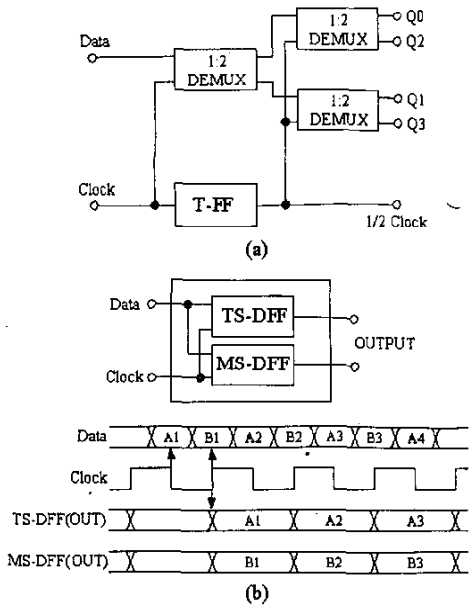

Figure 2. 1:4 DEMUX IC. (a) 1:4 DEMUX architecture. (b) 1:2 DEMUX block and the timing chart.

master-slave D flip-flop (MS-DFF), and selector (SEL) gate to ensure a wide phase margin, as shown in the timing chart. In order to achieve over 40 Gbit/s high-speed operation in the final 2:1 MUX stage, an emitter-coupled logic (ECL) series gate is used for the flip-flops. The ECL series gate technique can extract the full measure of device speed performance of our HBTs. In order to achieve low-power consumption in 4:2 MUX stages, a current-mode logic (CML) series gate is adopted for the flip-flops. In this paper, the flip-flop, which consists of current switches and emitter followers is called the ECL-type flip-flop. The flip-flop, which consists of current switches is called the CML-type flip-flop. The collector current densities of the CML-type flip-flop were designed to be about half that of the ECL-type flip-flop to reduce the power consumption as much as possible. The power consumption of the CML-type flip-flop is about 1/4 that of the ECL-type flip-flop. The internal voltage swing is designed to be 0.5 V for both flip-flops.

Another key blocks to achieve both high-speed operation and low-power consumption are the clock distribution circuits. Since there is a trade-off between the driving capability and the power consumption, we optimized the current density of each transistor in the clock distribution circuit by

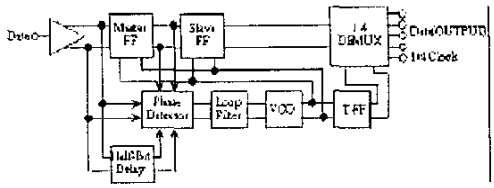

Figure 3. One-chip 1:4 DEMUX with CDR architecture.

determining the required operating speed and number of fan-outs. In optimizing the current density, we also took the parasitic resistances and capacitances of interconnecting metal layers into consideration. The parasitics were extracted from the layout patterns and back-annotated in the design cycle. The collector current densities were designed to be in the range of 50 to 100 kA/cm^2.

B. 1:4 DEMUX

A block diagram of the 1:4 DEMUX is shown in Fig. 2. The 1:4 DEMUX also employs the conventional tree-type architecture. The 1:2 DEMUX consists of a TS-DFF and MS-DFF. As shown in the timing chart in Fig. 3, a wide phase margin can be obtained by this architecture. The 1:2 DEMUX and the 2:4 DEMUX stages use flip-flops based on ECL and CML series gates, respectively. The collector current densities of each transistor for the clock distribution circuits in the 1:4 DEMUX are also optimized.

C. 1:4 DEMUX with CDR

The one-chip 1:4 DEMUX with CDR monolithically integrates a linear-type phase detector (PD), a lag-lead low-pass filter (LPF), full rate voltage-controlled oscillator (VCO), and 1:4 DEMUX as shown in Fig. 3. The 1:4 DEMUX mentioned above is used as the DEMUX in this IC. The linear-type PD enables low-power operation because it can be constructed with few transistors compare with other types of PDs. This IC operates at the full clock rate of 40 GHz. The IC consists of 531 transistors and 368 resistors.

Photographs of the 4:1 MUX, 1:4 DEMUX, and 1:4 DEMUX with the CDR are shown in Fig. 4. The chip size is 3 x 3 mm^2 for all ICs. The power supply voltage was designed to be –4.5 V.

III. FABRICATION TECHNOLOGY

The undoped-emitter InP/InGaAs HBTs used in this work were grown by metalorganic vapor phase epitaxy (MOVPE) on a 3-inch semi-insulating InP substrate. Carbon was the base dopant. We employed a simple non-self-aligned process to make these ICs

[8]. The HBT has a 70-nm-thick undoped InP emitter, a 50-nm-thick carbon-doped InGaAs base, and a 300-nm-thick InGaAs collector. The f_t and maximum oscillation frequency f_{max} were about 150 GHz and 200 GHz at a collector current density of 50 kA/cm^2 and a collector-to-emitter voltage of 1.2 V. In this work, all transistors have an emitter width of 1.0 um.

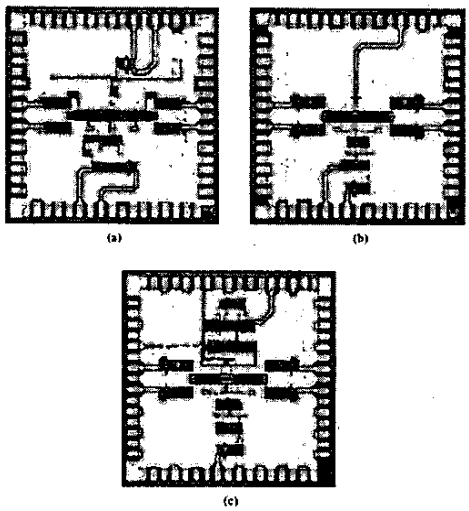

Figure 4. Photographs of the (a) 4:1 MUX, (b) 1:4 DEMUX, and (c) 1:4 DEMUX with the CDR.

IV. IC PERFORMANCE

Measurements of ICs were performed on-wafer using RF probes. For measurement of the 4:1 MUX, input data signals with word length of 2^{31}-1 were generated by a 4-channel pulse-pattern generator (PPG). The output data signal of the device under test (DUT) were demultiplexed into 4-channel data signals using a demultiplexer module consisting of GaAs MESFET and InP HEMT ICs [10]. Error-free operations were confirmed at every channel by using a 4-channel error detector. For measurement of the 1:4 DEMUX and 1:4 DEMUX with the CDR, we generated a pseudorandom bit stream (PRBS) up to 50 Gbit/s by quadrupling the PRBS of up to 12.5 Gbit/s with word length of 2^{31}-1 using a multiplexer module consisting of GaAs MESFET and InP HEMT ICs. We have confirmed the error-free operations of every channel in this case, too.

The 4:1 MUX was operated up to 50 Gbit/s. The dead bands were not observed. The clock phase margins were about 200 and 180 degrees at 45 and 50 Gbit/s, respectively. These phase margins include the skew for the 4-channel input data signals. The output pattern showed good eye opening at 50 Gbit/s (Fig. 5). The 1:4 DEMUX was operated at up to 50 Gbit/s. Fig. 6 is the demultiplexed output eye patterns at 50 Gbit/s. The clock phase margin was about 140 degree at 50 Gbit/s. The 1:4 DEMUX with the CDR was operated at 40 Gbit/s. The 1/4 clock signal and the demultiplexed output eye patterns are shown in Fig. 7. To our knowledge, this is the first demonstration of a 1:4 DEMUX with a CDR operating at the full clock rate of 40 GHz.

Low power consumptions of about 2.5, 2.6, and 3.6 W were achieved for the 4:1 MUX, 1:4 DEMUX, and 1:4 DEMUX with the CDR, respectively. It can be also said by our results that a 4:1 MUX with a clock multiplier unit (CMU) circuit will be achievable by using the 4:1 MUX and the

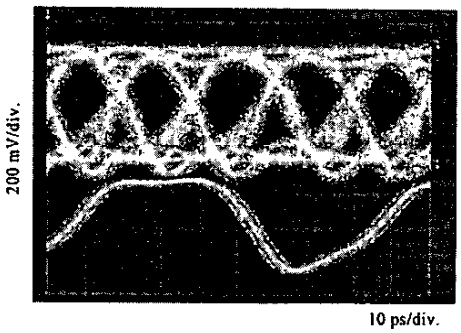

Figure 5. Output eye pattern of the 4:1 MUX at 50 Gbit/s (upper) and output clock signal (lower).

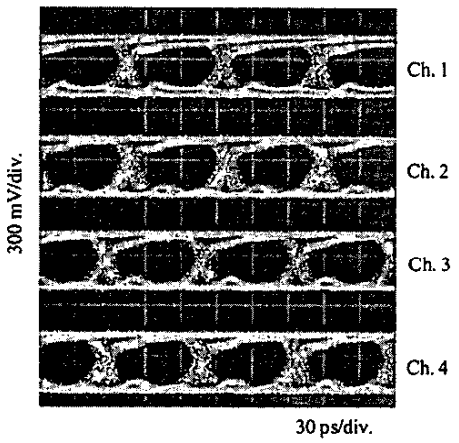

Figure 6. Output eye patterns of the 1:4 DEMUX at 50 Gbit/s.

phase-locked loop (PLL) architecture of the CDR circuit in this work.

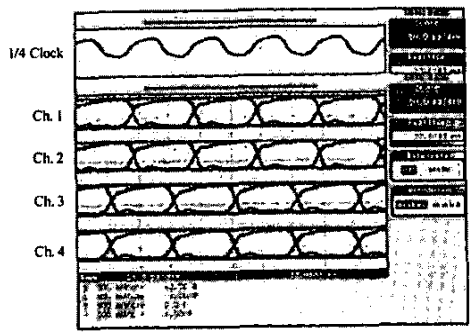

Figure 7. 1/4 output clock signal (upper) and output eye patterns of the 1:4 DEMUX with the CDR at 40 Gbit/s.

V. CONCLUSION

We have successfully designed and fabricated low-power 4:1 MUX, 1:4 DEMUX, and 1:4 DEMUX with CDR using undoped-emitter InP/InGaAs HBT technology. Up to 50 Gbit/s error-free operations were confirmed for the 4:1 MUX and 1:4 DEMUX, respectively. A 40-Gbit/s full-clock-rate operation for the 1:4 DEMUX with a CDR was achieved. The results of our work demonstrate that undoped-emitter InP/InGaAs HBT technology is an excellent choice for fabricating high-speed low-power ICs for optical communications systems and measuring equipment operating at bit rates of over 40 Gbit/s.

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